ByteBlasterMV Parallel Port Download Cable

April 1998, ver. 1 Data Sheet

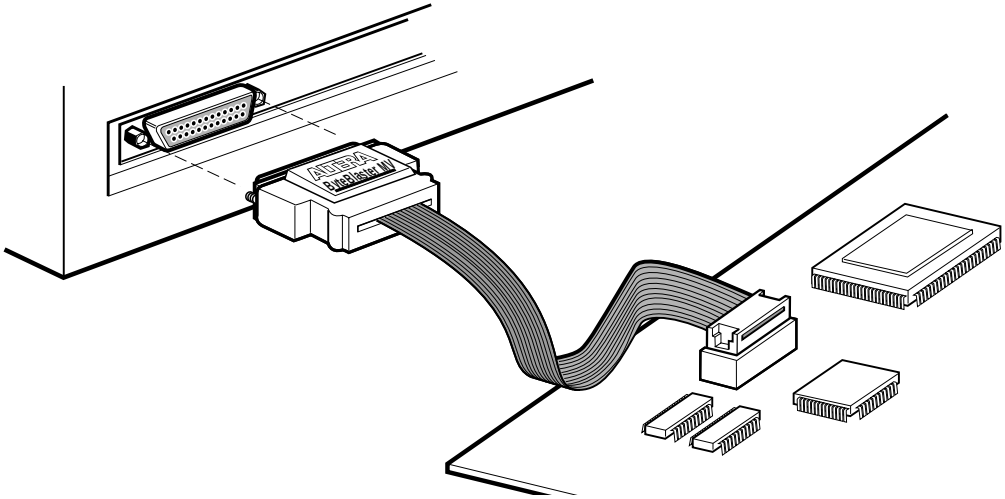
Features

- Allows PC users to perform the following functions:
  - Program MAX® 9000, MAX 7000S, and MAX 7000A devices in-system via a standard parallel port
  - Configure FLEX® 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, and FLEX 6000 devices
- Supports operation while powered up with V_{CC} at 3.3 V or 5.0 V
- Provides a fast and low-cost method for in-system programming
- Downloads data from the MAX+PLUS® II development software
- Interfaces with a standard 25-pin parallel port on PCs
- Uses a 10-pin circuit board connector, which is identical to that of the ByteBlaster™ parallel port and BitBlaster™ serial download cables

Functional Description

The ByteBlasterMV™ parallel port download cable (ordering code: PL-BYTEBLASTERMV) is a hardware interface to a standard PC parallel port (also known as an LPT port). This cable drives configuration data to FLEX 10K (including FLEX 10KA and FLEX 10KE), FLEX 8000, and FLEX 6000 devices, as well as programming data to MAX 9000, MAX 7000S, and MAX 7000A devices. Because design changes are downloaded directly to the device, prototyping is easy and multiple design iterations can be accomplished in quick succession. See Figure 1.

Figure 1. ByteBlasterMV Parallel Port Download Cable



A-DS-BYTBLMV-01
L01-05942-00

Download Modes

The ByteBlasterMV cable provides two download modes:

- Passive serial (PS) mode—Used for configuring FLEX 10K, FLEX 8000, and FLEX 6000 devices
- JTAG mode—Industry-standard Joint Test Action Group (JTAG) interface for programming or configuring FLEX 10K, MAX 9000, MAX 7000S, and MAX 7000A devices

ByteBlasterMV Connections

The ByteBlasterMV cable has a 25-pin male header that connects to the PC parallel port, and a 10-pin female plug that connects to the circuit board. Data is downloaded from the PC's parallel port through the ByteBlasterMV cable to the circuit board via the connections discussed in this section.

To configure 2.5-V FLEX 10KE devices using the ByteBlasterMV download cable, connect the pull-up resistors to a 3.3-V power supply, the cable's VCC pin to a 3.3-V power supply, and the device's VCCINT pin to a 2.5-V power supply. For PS configuration, the device's VCCIO pin must be connected to a 2.5-V or 3.3-V power supply; for JTAG configuration, the device's VCCIO pin must be connected to a 3.3-V power supply. Because FLEX 10KE devices have 3.3-V and 5.0-V tolerant inputs, they will configure successfully with the cable's 3.3-V output.

ByteBlasterMV Header & Plug Connections

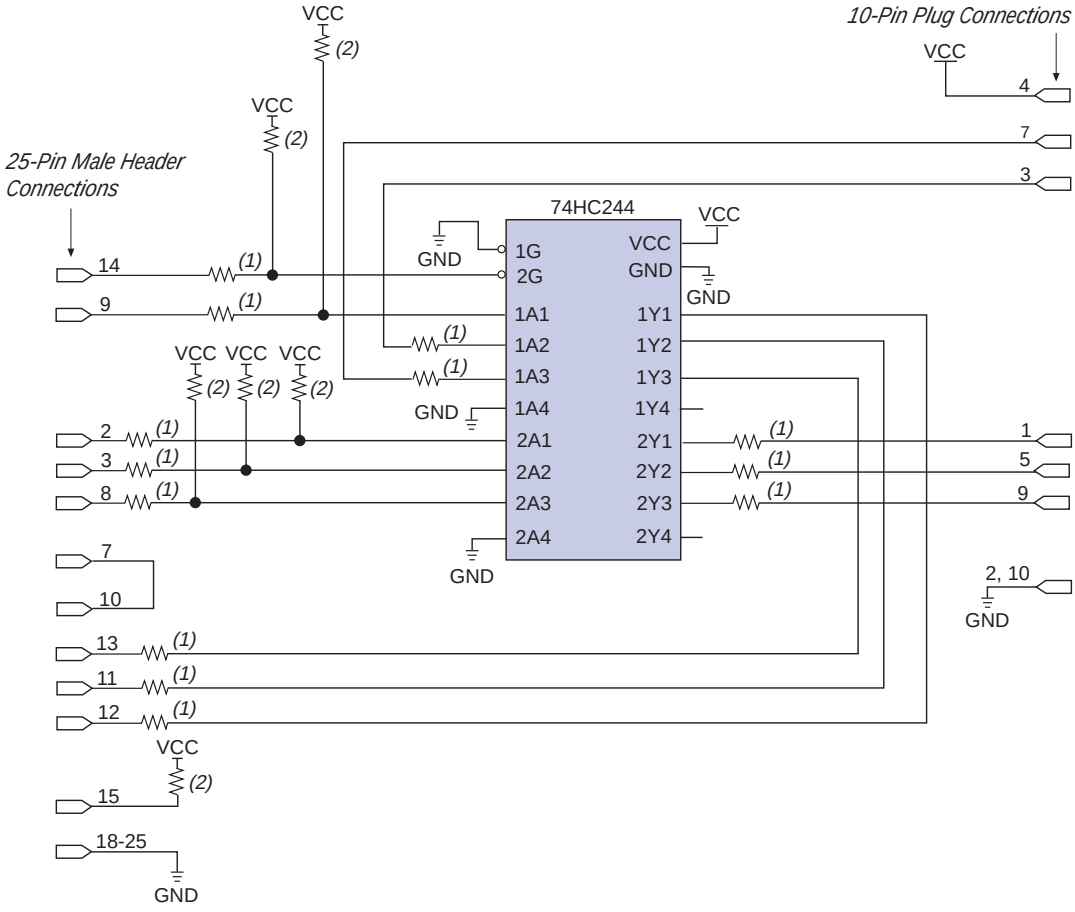
The 25-pin male header connects to a parallel port with a standard parallel cable. Table 1 identifies the pins and the download modes.

Table 1. ByteBlasterMV 25-Pin Header Pin-Outs

Pin	PS Mode Signal Name	JTAG Mode Signal Name
2	DCLK	TCK
3	nCONFIG	TMS
8	DATA0	TDI
11	CONF_DONE	TDO
13	nSTATUS	–
15	VCC	VCC
18 to 25	GND	GND

Figure 2 shows a schematic of the ByteBlasterMV download cable.

Figure 2. ByteBlasterMV Schematic



Notes:
(1) All series resistors are 100 Ω.
(2) All pull-up resistors are 2.2 KΩ.

The 10-pin female plug connects to a 10-pin male header on the circuit board containing the target device(s). Figure 3 shows the dimensions of the female plug.

Figure 3. ByteBlasterMV 10-Pin Female Plug Dimensions

Dimensions are shown in inches. The spacing between pin centers is 0.1 inch.

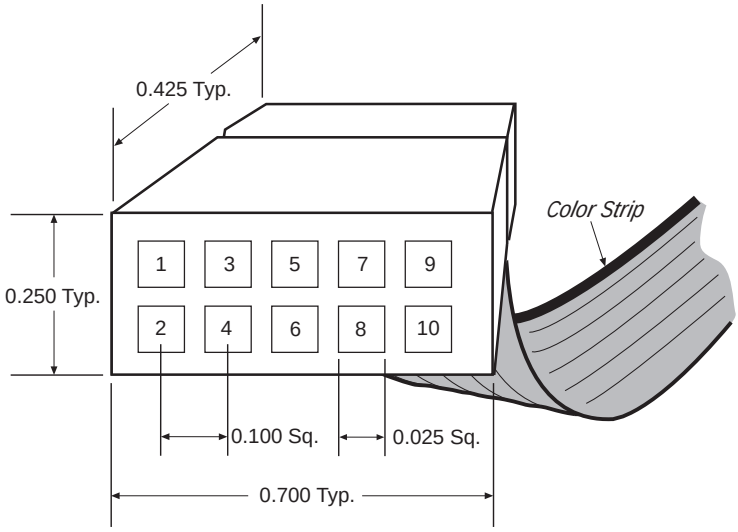


Table 2 identifies the 10-pin female plug's pin names for the corresponding download mode.

Table 2. ByteBlasterMV Female Plug's Pin Names & Download Modes

Pin	PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description
1	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration control	TDO	Data from device
4	VCC	Power supply	VCC	Power supply
5	nCONFIG	Configuration control	TMS	JTAG state machine control
6	–	No connect	–	No connect
7	nSTATUS	Configuration status	–	No connect
8	–	No connect	–	No connect
9	DATA0	Data to device	TDI	Data to device
10	GND	Signal ground	GND	Signal ground

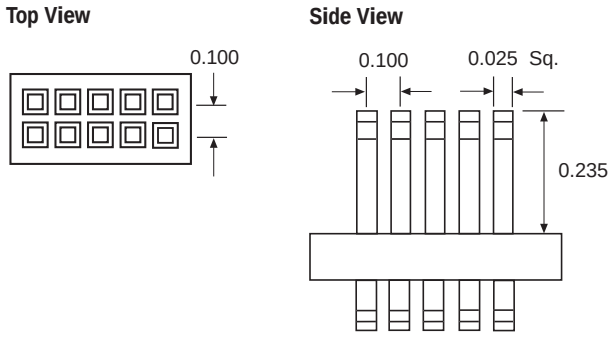
The circuit board must supply V_{CC} and ground to the ByteBlasterMV cable.

Circuit Board Header Connection

The ByteBlasterMV 10-pin female plug connects to a 10-pin male header on the circuit board. The 10-pin male header has two rows of five pins, which are connected to the device's programming or configuration pins. The ByteBlasterMV cable receives power and downloads data via the male header. Figure 4 shows the dimensions of a typical 10-pin male header.

Figure 4. 10-Pin Male Header Dimensions

Dimensions are shown in inches.



Operating Conditions

The following tables summarize the absolute maximum ratings, recommended operating conditions, and DC operating conditions for the ByteBlasterMV cable.

ByteBlasterMV Cable Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground	–0.5	7.0	V
V_I	DC input voltage	With respect to ground	–0.5	7.0	V

ByteBlasterMV Cable Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage, 5.0-V operation		4.5	5.5	V
	Supply voltage, 3.3-V operation		3.0	3.6	V

ByteBlasterMV Cable DC Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	V_{CC} = 4.5 V	3.15		V
		V_{CC} = 3.0 V	2.1		
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V		1.35	V
		V_{CC} = 3.0 V		0.9	
V_{OH}	5.0-V high-level TTL output voltage	TTL load. V_{CC} = 4.5 V, I_{OH} = 8 mA	3.80		V
	3.3-V high-level TTL output voltage	TTL load. V_{CC} = 3.0 V, I_{OH} = 4 mA	2.48		V
	5.0-V high-level CMOS output voltage	CMOS load. V_{CC} = 4.5 V, I_{OH} = 50 µA	4.4		V
	3.3-V high-level CMOS output voltage	CMOS load. V_{CC} = 3.0 V, I_{OH} = 50 µA	2.9		V
V_{OL}	5.0-V low-level TTL output voltage	TTL load. V_{CC} = 4.5 V, I_{OL} = 8 mA		0.44	V
	3.3-V low-level TTL output voltage	TTL load. V_{CC} = 3.0 V, I_{OL} = 4 mA		0.44	V
	5.0-V low-level CMOS output voltage	CMOS load. V_{CC} = 4.5 V, I_{OL} = 50 µA		0.1	V
	3.3-V low-level CMOS output voltage	CMOS load. V_{CC} = 3.0 V, I_{OL} = 50 µA		0.1	V
I_{CC}	Operating current			50	mA

Passive Serial Mode

This section discusses PS configuration for single and multiple FLEX devices. In PS configuration, the data is sent to the FLEX device serially by the data source; in this case, the data source is the ByteBlasterMV cable. The data is synchronized to a clock that is supplied by the data source.

PS Configuration of a Single FLEX Device

Single FLEX devices can be configured using PS configuration and the MAX+PLUS II Programmer. Devices are configured with an SRAM Object File (**.sof**), generated automatically during project compilation. For more information, go to "Software Instructions" on page 14.

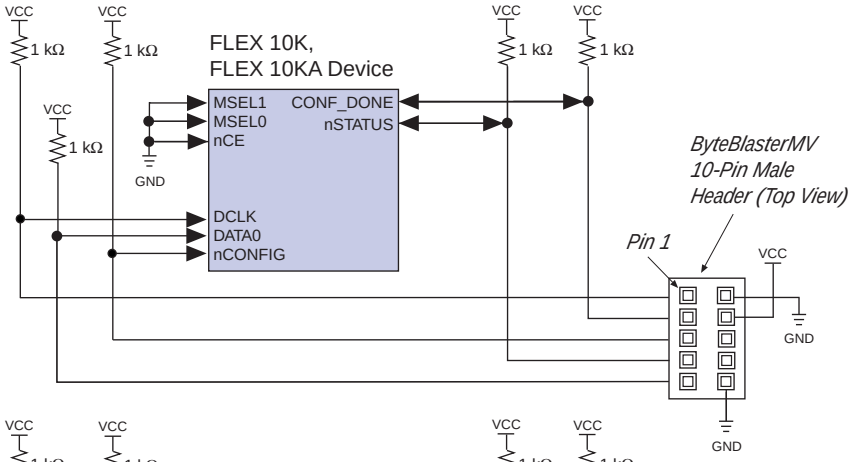
Figure 5 shows how the ByteBlasterMV cable interfaces with a single FLEX device. If the DATA0 pin is used in user mode, it must be isolated during configuration.

Go to the following sources for additional information:

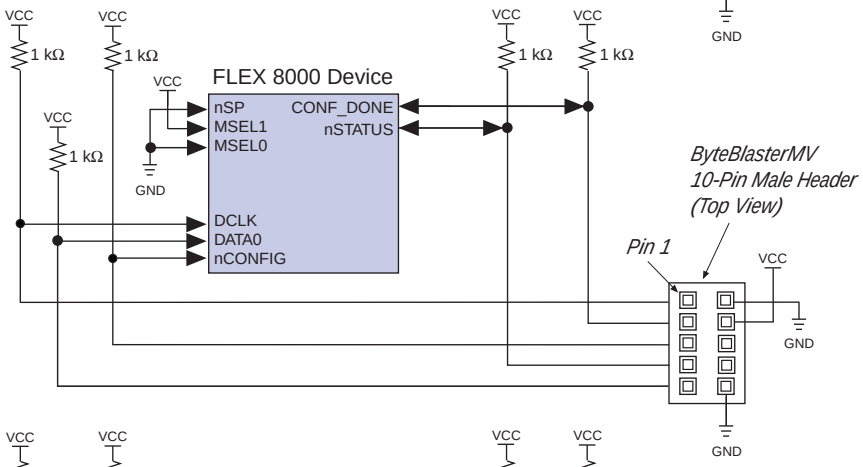
- *Application Note 59 (Configuring FLEX 10K Devices)*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
- *Application Note 87 (Configuring FLEX 6000 Devices)*
- Search for "Configuring a Single Device with the BitBlaster, ByteBlaster, or FLEX Download Cable" in MAX+PLUS II Help

Figure 5. Single FLEX Device Configuration with the ByteBlasterMV Cable

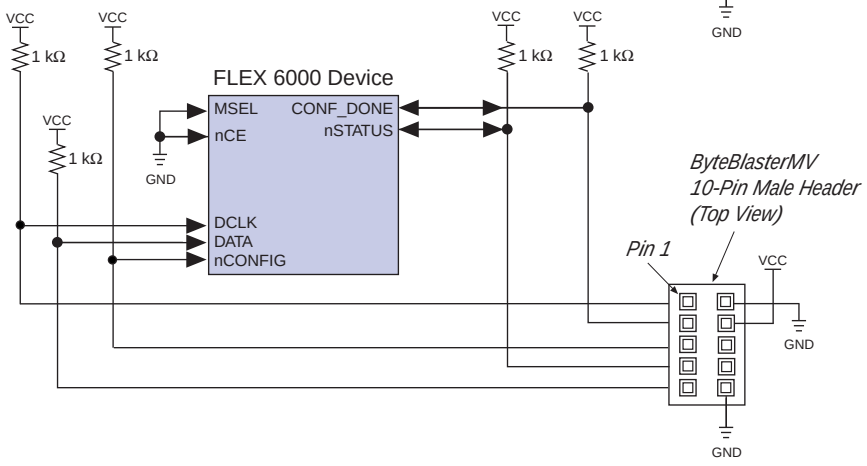
FLEX 10K, FLEX 10KA Device



FLEX 8000 Device



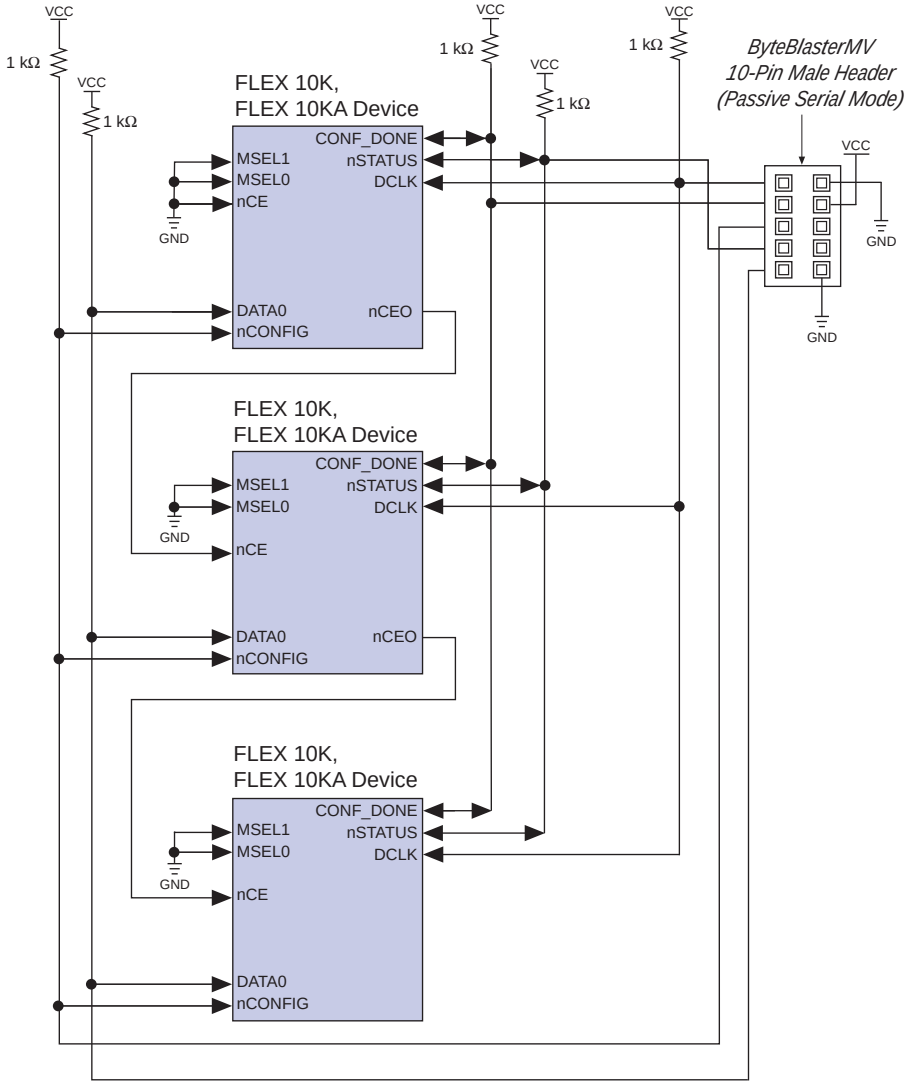
FLEX 6000 Device



PS Configuration of Multiple FLEX Devices

Multiple FLEX 10K, FLEX 8000, or FLEX 6000 devices can be configured via the ByteBlasterMV cable in PS mode using the MAX+PLUS II Programmer. See Figures 6, 7, and 8.

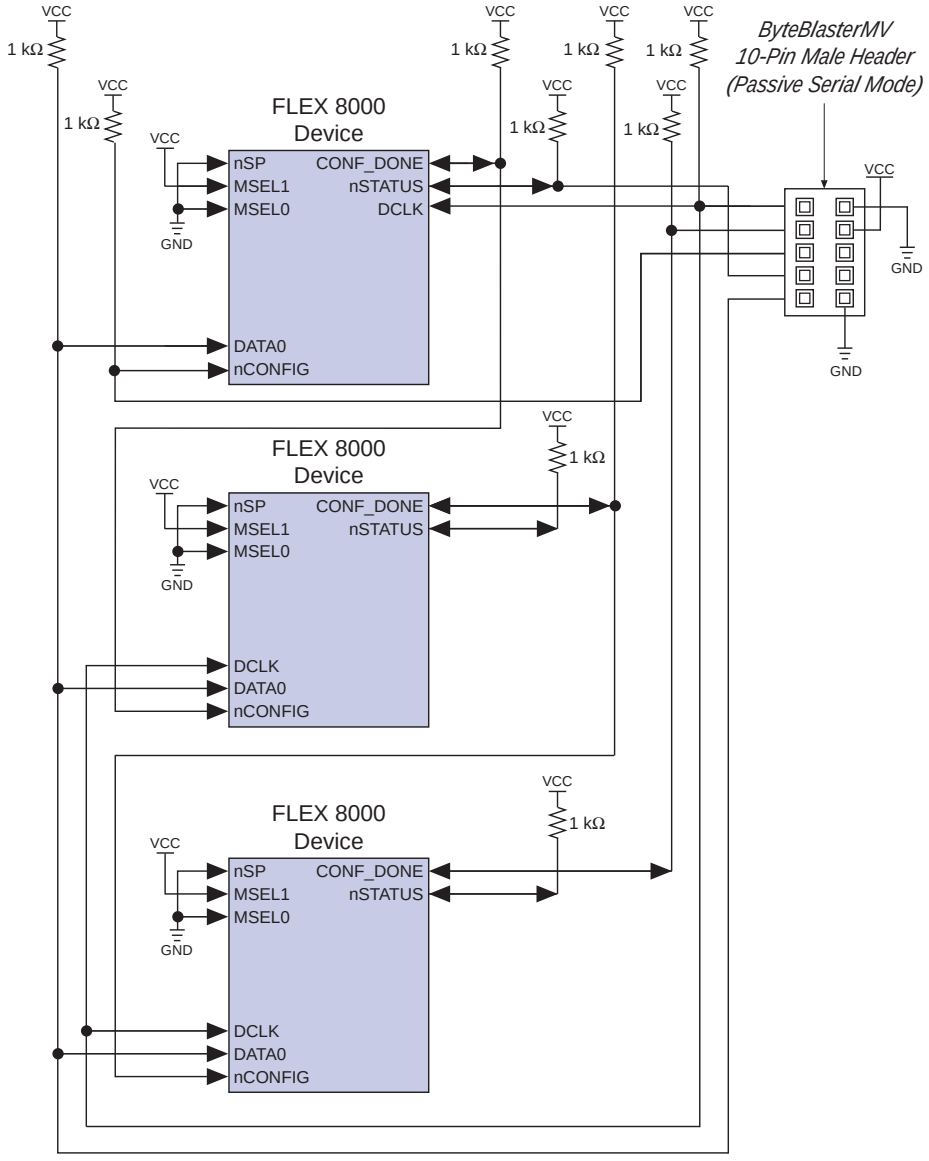
Figure 6. FLEX 10K & FLEX 10KA Multi-Device PS Configuration with the ByteBlasterMV Cable *Note (1)*



Note:

(1) When more than five devices are connected in a PS chain, Altera recommends buffering the DCLK and DATA pins.

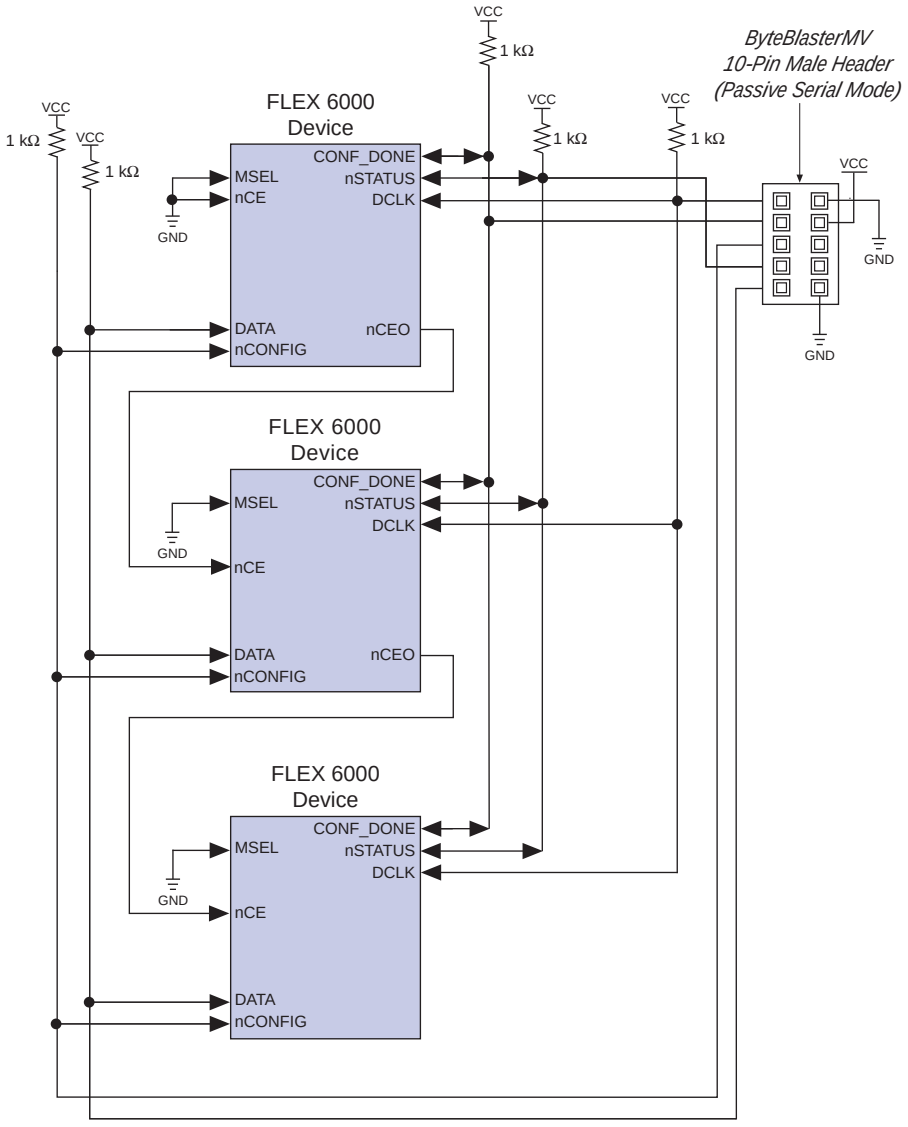
Figure 7. FLEX 8000 Multi-Device PS Configuration with the ByteBlasterMV Cable *Note (1)*



Note:

(1) When more than five devices are connected in a PS chain, Altera recommends buffering the DCLK and DATA pins.

Figure 8. FLEX 6000 Multi-Device PS Configuration with the ByteBlasterMV Cable *Note (1)*



Note:

(1) When more than five devices are connected in a PS chain, Altera recommends buffering the DCLK and DATA pins.

FLEX 10K and FLEX 6000 devices can also be configured in the same configuration chain. The nCEO pin of a FLEX 10K device can be connected to the nCE pin of a FLEX 6000 device and vice versa. The CONF_DONE and nSTATUS pins of all the devices in the configuration chain must be tied together.

For more information, search for "Configuring Multiple FLEX Devices in a FLEX Chain with the BitBlaster, ByteBlaster, or FLEX Download Cable" in MAX+PLUS II Help.

JTAG Mode

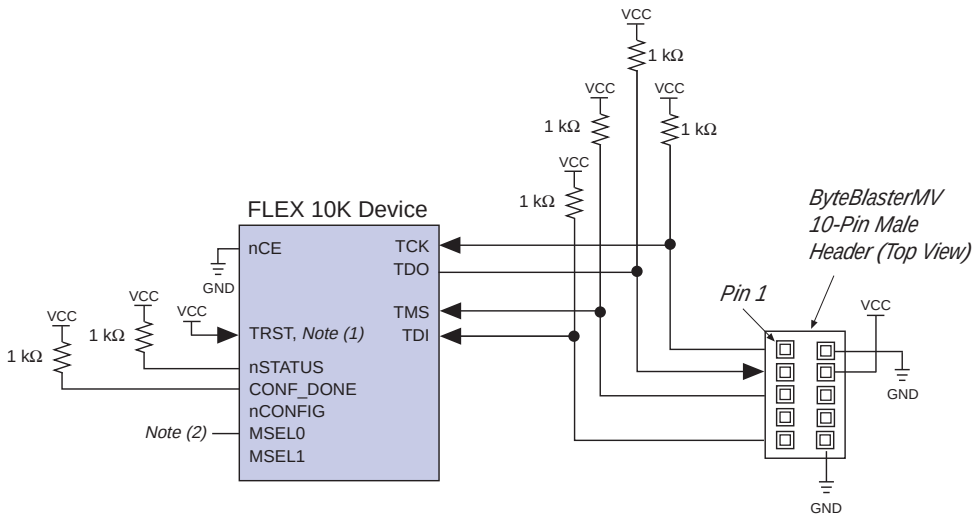
For in-system programming and in-circuit reconfiguration in JTAG mode, the ByteBlasterMV cable connects to devices on the circuit board via any standard parallel port. This section discusses the following topics:

- JTAG configuration of a single FLEX 10K device
- JTAG programming of a single MAX 9000, MAX 7000S, or MAX 7000A device
- JTAG programming and configuration of multiple devices

JTAG Configuration of a Single FLEX 10K Device

The MAX+PLUS II software downloads the SRAM Object File (**.sof**), created during compilation, directly to the FLEX 10K device via the ByteBlasterMV cable. Refer to "Software Instructions" on page 14 for more information. Devices are configured via the JTAG pins: TCK, TMS, TDI, and TDO. Figure 9 shows how the ByteBlasterMV cable interfaces with a single FLEX 10K device. All other I/O pins are tri-stated in this configuration.

Figure 9. JTAG Configuration of a Single FLEX 10K Device



Notes:

(1) FLEX 10K devices in 144-pin thin quad flat pack (TQFP) packages do not have a TRST pin. Therefore, the TRST pin can be ignored when using these devices.

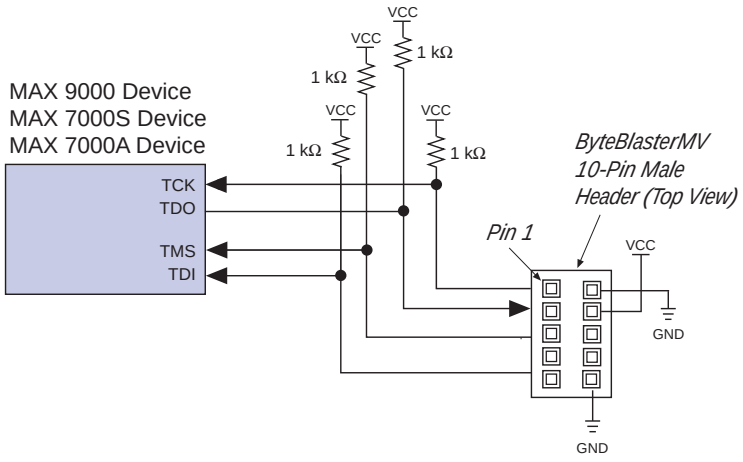
(2) The nCONFIG, MSEL0, and MSEL1 pins should be connected to support a FLEX configuration scheme. If only JTAG configuration is used, connect nCONFIG to V_{CC}, and MSEL0 and MSEL1 to ground.

JTAG Programming of a Single MAX 9000, MAX 7000S or MAX 7000A Device

The MAX+PLUS II software downloads the Programmer Object File (**.pof**) created during compilation directly to the MAX device via the ByteBlasterMV cable. Refer to "Software Instructions" on page 14 in this data sheet for more information.

Devices are programmed via the device JTAG pins: TCK, TMS, TDI, and TDO. Figure 10 shows how the ByteBlasterMV cable interfaces with a MAX 9000, MAX 7000S, or MAX 7000A device. The I/O pins are tri-stated during in-system programming.

Figure 10. MAX 9000, MAX 7000S & MAX 7000A Device Programming with the ByteBlasterMV Cable



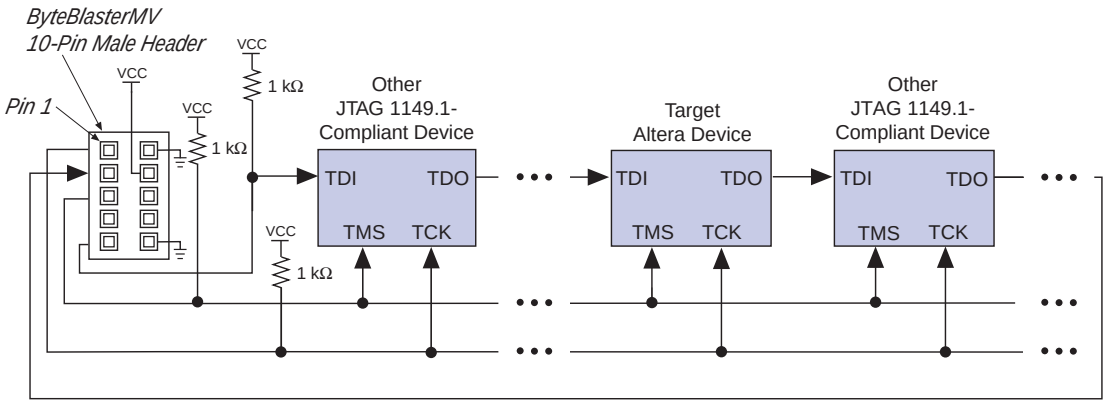
Search for "Programming a Single Device with the BitBlaster or ByteBlaster" in MAX+PLUS II Help for more information.

JTAG Programming & Configuration of Multiple Devices

When programming a JTAG chain of devices, one JTAG-compatible plug, such as the ByteBlasterMV 10-pin female plug, is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the ByteBlasterMV cable. Refer to "ByteBlasterMV Cable DC Operating Conditions" on page 6. However, when more than 5 devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins.

JTAG-chain device programming is ideal when the circuit board contains multiple devices, or when the circuit board is tested using JTAG boundary-scan testing. Refer to Figure 11.

Figure 11. JTAG-Chain Device Programming & Configuration with the ByteBlasterMV Cable



If FLEX 10K devices are part of the JTAG configuration chain, the nCONFIG, MSEL0, MSEL1, CONF_DONE, and nSTATUS pins should be connected as shown in Figure 9; this setup only applies when a JTAG configuration scheme is used, i.e., not when a combination of FLEX and JTAG configuration schemes are used. The CONF_DONE and nSTATUS pins on each device should be pulled-up independently.

FLEX 10K devices in 144-pin TQFP packages do not have a TRST pin. Therefore, the TRST pin can be ignored when configuring multiple FLEX 10K 144-pin TQFP devices.

To program a single device in a JTAG chain, the programming software places all other devices (including non-Altera devices) in the JTAG chain in BYPASS mode. In BYPASS mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally, thereby enabling the programming software to program or verify the target device.

MAX 9000, MAX 7000S, and MAX 7000A devices can be programmed in-system using a JTAG chain; FLEX 10K devices can be configured in-circuit using a JTAG chain. In addition, MAX and FLEX devices can be placed within the same JTAG chain for device programming and configuration. See Figure 11.

Go to the following sources for additional information:

- *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- Search for "Setting Up Multi-Device JTAG Chains," "Configuring Multiple Devices in a JTAG Chain with the BitBlaster or ByteBlaster," and "Programming Multiple Devices in a JTAG Chain with the BitBlaster or ByteBlaster" in MAX+PLUS II Help.

Software Instructions

The MAX+PLUS II Programmer downloads configuration or programming data for FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000S, or MAX 7000A devices.

To configure or program one or more devices with the ByteBlasterMV cable and the MAX+PLUS II Programmer, follow these steps:

1. Compile a project. The MAX+PLUS II Compiler automatically generates an SOF for FLEX 10K, FLEX 8000, and FLEX 6000 device configuration, or a POF for MAX 9000, MAX 7000S, and MAX 7000A device programming.

2. Attach the ByteBlasterMV cable to a parallel port on a PC and insert the 10-pin female plug into the prototype system containing the target device. The board must supply power to the ByteBlasterMV cable.

For the Windows NT operating system, a driver must be installed before using the ByteBlasterMV cable. Go to the *MAX+PLUS II Getting Started Manual* for instructions on installing ByteBlasterMV drivers.

3. Open the MAX+PLUS II Programmer. Choose the **Hardware Setup** command (Options menu) to specify the ByteBlasterMV cable and the appropriate LPT port. See "Changing the Hardware Setup" in MAX+PLUS II Help for more information.

The MAX+PLUS II software automatically loads the programming file for the current project (either a POF or SOF), or the first programming file for a multi-device project. To specify another programming file, choose **Select Programming File** (File menu) and specify the correct file. For a FLEX 10K, FLEX 8000, or FLEX 6000 device, select an SOF; for a MAX 9000, MAX 7000S, or MAX 7000A device, select a POF.

4. For JTAG or FLEX-chain programming or configuration, perform the following steps:

   ✓ To program or configure devices in a JTAG chain (multi- or single-device chain), turn on **Multi-Device JTAG-Chain** (JTAG menu) and choose **Multi-Device JTAG Chain Setup** to set up the multi-device JTAG chain. See "Setting up Multi-Device JTAG Chains" in MAX+PLUS II Help for more information.

   ☞ If the JTAG chain includes either FLEX or MAX devices exclusively, set up and create just one JTAG Chain File (**.jcf**). Likewise, if the JTAG chain includes a mixture of FLEX and MAX devices, set up and create two separate JCFs. One JCF will configure the FLEX devices, and the other JCF will program the MAX devices.

   ✓ To configure multiple devices in a FLEX chain, turn on **Multi-Device FLEX Chain** (FLEX menu) and choose **Multi-Device FLEX Chain Setup** to set up the multi-device FLEX chain. See "Setting Up Multi-Device FLEX Chains" in MAX+PLUS II Help for more information.

5. Choose the **Program** or **Configure** button to program or configure the device(s).

The ByteBlasterMV cable downloads the data from the SOF or POF File(s) into the device(s).

Conclusion

Downloading configuration and programming data directly to the device via the ByteBlasterMV cable allows designers to verify multiple design iterations in quick succession, thereby speeding the design cycle.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
(888) 3-ALTERA
lit_req@altera.com